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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/364,727	07/30/1999	STEPHEN L. SCARINGELLA	E0295/7126WR	9805

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EXAMINER
ORTIZ JR., BENJAMIN

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/364,727	SCARINGELLA ET AL.	
	Examiner	Art Unit	
	Benjamin Ortiz Jr.	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-4,6 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorfman et al. U.S. Patent No. 6,118,862 in view of Don et al. U.S. Patent No. 6,266,740. Referring to claims 1,6,12 and 13, Dorfman et al. discloses a computer system that includes a circuit board, specifically a processor board that has a processor, a memory and a disk controller (column 4, line 17). The system also includes a backplane that has a plurality of slots that are adapted to accept plug-in boards (column 4, lines 30-33). In the system, the processor board is adapted to be received into a slot on the backplane establishing a connection between the processor board and the backplane (column 4, line 42). It is also disclosed that the processor board is in communication with any devices (such as circuit boards) that are installed in the available slots of the backplane (column 4, line 44). Dorfman et al. does not disclose storing product data of the processor board on the memory. However, Don et al. teaches a method that establishes a memory space within local memory for storing ID data (ID codes), such as cabinet serial number, device number, among others (column 5, line 54). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify Dorfman's

invention to include product data on the memory that is included on the processor boards in order for each board to have its own unique identification means.

Referring to claims 2-4 and 14, Dorfman et al. further teaches the use of a read only memory (ROM) on the processor boards in his system (column 4, line 22). Also, it is well known in the art that other types of ROM can be used such as EEPROMs among other types of ROM.

2. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dorfman et al. in view of Don et al. as applied to claim 1, and further in view of. Wilhelm U.S. Patent No. 5,761,033. Dorfman et al., as modified, discloses a computer system that includes a circuit board, specifically a processor board that has a processor, a memory (ROM) and a disk controller. Product data is stored in the ROM on included in the circuit board. The system also includes a backplane that has a plurality of slots that are adapted to accept plug-in boards. In the system, the processor board is adapted to be received into a slot on the backplane establishing a connection between the processor board and the backplane. Dorfman does not disclose that external access is provided, via the backplane, to the circuit boards that are installed in the plurality of slots of the backplane. However, Wilhelm teaches a system where external access is provided via bus receptacles on a backplane. The backplane has a plurality of bus lines interconnecting the bus receptacles and forming a system bus for carrying power, address, data and other signals (column 9, lines 34-39). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify Dorfman's invention to include such a backplane in order to provide external access to the backplane and, there forth, providing external access to the devices installed on the backplane.

3. Claims 7-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorfman et al. in view of Don et al. as applied to claim 1. Referring to claims 7 and 11, Dorfman et al., as modified, discloses a computer system that includes a circuit board, specifically a processor board that has a processor, a memory (ROM) and a disk controller. Product data is stored in the ROM on included in the circuit board. The system also includes a backplane that has a plurality of slots that are adapted to accept plug-in boards. In the system, the processor board is adapted to be received into a slot on the backplane establishing a connection between the processor board and the backplane. It is also disclosed that the processor board is in communication with any devices (such as circuit boards) that are installed in the available slots of the backplane. Dorfman does not disclose the use of an array of storage devices or cache memory. However, Don et al. teaches the use of a global memory that serves as a very large cache, which is used as a staging area during the transfer of data between the host computer and the storage devices (disk arrays) that are used in his invention (column 3, line 55). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify Dorfman's invention to include such a global memory that includes cache memory in order for the circuit boards to have a staging area to control data transfers between the host computer and the storage devices (disk arrays).

Referring to claims 8 and 9, Dorfman et al. further teaches the use of a read only memory (ROM) on the processor boards in his system (column 4, line 22). Also, it is well known in the art that other types of ROM can be used such as EEPROMs among other types of ROM.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dorfman et al. in view of Don et al. as applied to claim 7, and further in view of. Wilhelm. Dorfman et al., as modified, discloses a computer system that includes a circuit board, specifically a processor board that has a processor, a memory (ROM) and a disk controller. Product data is stored in the ROM on included in the circuit board. The system also includes a backplane that has a plurality of slots that are adapted to accept plug-in boards. In the system, the processor board is adapted to be received into a slot on the backplane establishing a connection between the processor board and the backplane. It is also disclosed that the processor board is in communication with any devices (such as circuit boards) that are installed in the available slots of the backplane. Dorfman does not disclose that external access is provided, via the backplane, to the circuit boards that are installed in the plurality of slots of the backplane. However, Wilhelm teaches a system where external access is provided via bus receptacles on a backplane. The backplane has a plurality of bus lines interconnecting the bus receptacles and forming a system bus for carrying power, address, data and other signals (column 9, lines 34-39). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify Dorfman's invention to include such a backplane in order to provide external access to the backplane and, there forth, providing external access to the devices installed on the backplane.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to circuit boards having on board memory storing product data:

a. U.S. Patent No. 5,177,744 to Cesare et al., which discloses a method and apparatus for error recovery in arrays.

b. U.S. Patent No. 6,154,854 to Stallmo, which discloses a logical partitioning of a redundant array storage system.

c. U.S. Patent No. 4,633,412 to Ebert, Jr. et al., which discloses an option protocol arrangement for stored program rectifier controller.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin Ortiz Jr. whose telephone number is (703)305-3844. The examiner can normally be reached on Mon-Fri 8:00am-5:30pm, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Wong can be reached on (703)305-3477. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7239 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

bo
October 28, 2002

XUAN M. THAI
PRIMARY EXAMINER
TC 2100